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VLSI Projects in combining multiple transistors in a chip. All modern chips employ VLSI Architecture Design. VLSI is a technology by which 10000-1 Million Transistors can be fabricated on a single chip. VLSI in short is a Computer microchip miniaturization. **Software used in VLSI Projects** is Xilinx, Tanner Tool pro, Altera.

We assist research Scholars in implementing **VLSI Projects** with best Customer Support. For more details contact us: +91 9790238391.

DOMAIN AREA:

- DSP.
- Robotics.
- Automobile.
- Data Communication networks.
- Digital Signal Processing.

STEPS in VLSI Projects

- Specify functional design (Behavioral Simulation).
- Register transfer level design (RTL Simulation).
- Logic design (Logic Simulation).
- Circuit design (Timing Simulation).
- Physical design (Design rule checking).

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Sample IEEE VLSI Projects Topics

SI	Top 50 2015 IEEE VLSI Projects Titles.
1	The Diffusion Network in Analog VLSI Exploiting Noise-Induced Stochastic Dynamics to Regenerate Various Continuous Paths.
2	VLSI implementation of coupled MRF model using pulse-coupled phase oscillators.
3	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications.
4	Nonsmooth Optimization Method for VLSI Global Placement.
5	Crosstalk noise and delay analysis for high speed on-chip global RLC VLSI interconnects with mutual inductance using 90nm process technology.
6	A Nonlinear Analytical Optimization Method for Standard Cell Placement of VLSI Circuits.
7	Improvement in error resilience for compressed VLSI test data using Hamming code based technique.
8	High efficiency VLSI implementation of an edge-directed video up-scaler using high level synthesis.
9	High performance VLSI architecture for 2-D DWT using lifting scheme.
10	Low-Power VLSI Architectures for DCT/DWT: Precision vs Approximation for HD Video, Biomedical, and Smart Antenna Applications.
11	VLSI Design for SVM-Based Speaker Verification System.
12	An Efficient VLSI Architecture of a Reconfigurable Pulse-Shaping FIR Interpolation.
13	Digital VLSI Implementation of Piecewise-Affine Controllers Based on Lattice Approach.
14	Fully Pipelined Low-Cost and High-Quality Color Demosaicking VLSI Design for Real-Time Video Applications.
15	Unified VLSI architecture for photo core transform used in JPEG XR.
16	Design and VLSI implementation of novel pre-screening and simplified sorting based K-best detection for MIMO systems.
17	A VLSI Circuit Emulation of Chemical Synaptic Transmission Dynamics and Postsynaptic DNA Transcription.
18	A VLSI architecture for watermarking of grayscale images using weighted median prediction.
19	DEJA VU: An Entropy Reduced Hash Function for VLSI Layout Databases.
20	Modified SA algorithm for wirelength minimization in VLSI circuits.
21	VLSI Implementation of a Key Distribution Server Based Data Security Scheme for RFID System.
22	An optimum VLSI design of a 16-BIT ALU.
23	A High-Throughput VLSI Architecture for Hard and Soft SC-FDMA MIMO Detectors.
24	Ultra-High-Throughput VLSI Architecture of H.265/HEVC CABAC Encoder for UHDTV Applications.

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25	Energy Optimized Subthreshold VLSI Logic Family With Unbalanced Pull-Up/Down Network and Inverse Narrow-Width Techniques.
26	A novel approach for constrained via minimization problem in VLSI channel routing.
27	A review report on low power VLSI systems analysis and modeling techniques.
28	Revisiting Central Limit Theorem: Accurate Gaussian Random Number Generation in VLSI.
29	High-Throughput Power-Efficient VLSI Architecture of Fractional Motion Estimation for Ultra-HD HEVC Video Encoding.
30	An efficient VLSI architecture for fingerprint recognition using O2D-DWT architecture and modified CORDIC-FFT.
31	A Novel Area-Efficient VLSI Architecture for Recursion Computation in LTE Turbo Decoders.
32	Fast obstacle-avoiding octilinear steiner minimal tree construction algorithm for VLSI design.
33	Reconfiguration-Based VLSI Design for Security.
34	An algorithm for Via minimization in two layer channel routing of VLSI design.
35	VLSI implementation of efficient image watermarking algorithm.
36	Depth-Reliability-Based Stereo-Matching Algorithm and Its VLSI Architecture Design.
37	Cloud Computing For VLSI Floorplanning Considering Peak Temperature Reduction.
38	Neuromorphic VLSI second-order synapse.
39	Neuromorphic VLSI Bayesian integration synapse.
40	Energy Consumption of VLSI Decoders.
41	Internet of Things enabled green VLSI design on FPGA.
42	GFCG: Glitch free combinational clock gating approach in nanometer VLSI circuits.
43	Design and synthesis of bandwidth efficient QPSK modulator for low power VLSI design.
44	VLSI implementation of embedded back-end for photo-acoustic based continuous noninvasive blood glucose monitoring system.
45	Spintronics-based nonvolatile logic-in-memory architecture towards an ultra-low-power and highly reliable VLSI computing paradigm.
46	Novel VLSI architecture for real time medical image segmentation.
47	A New Parallel VLSI Architecture for Real-time Electrical Capacitance Tomography.
48	From the present to the future: Scaling of planar VLSI-CMOS devices towards 3D-FinFETs and beyond 10nm CMOS technologies; manufacturing challenges and future technology concepts.
49	VLSI-Assisted Nonrigid Registration Using Modified Demons Algorithm.
50	A strain-sensor-integrated test bed for electro mechanical characterization of VLSI probe.