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VHDL projects facilitate in designing mixed-signal circuits. Verilog concepts aid in design and verification of digital circuit at the register-transfer level. VHDL refers to Verilog Hardware Description Language. Xilinx Software is used in constructing VHDL Projects.

We assist research Scholars in implementing **VHDL Projects** with best Customer Support. For more details contact us: +91 9790238391.

Verilog HDL:

- Hardware description languages such as Verilog differ from software programming languages.
- Verilog is case-sensitive and has a basic preprocessor.
- Modules encapsulate design hierarchy.
- They communicate with other modules through a set of declared input, output, and bidirectional ports.

VHDL Projects.

- Easy to learn and easy to use.
- Allows describing various levels of abstractions without choosing a specific fabrication technology.
- Makes it easier to design large and complex systems.
- No need to manually place gates to build circuits.

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DOMAIN AREA:

- VLSI.
- Computer Networks.

STEPS Involved in VHDL Projects.

- Perform RTL functional simulation.
- Post-synthesis simulation.
- Gate-level timing simulation.

ABSTRACTION LEVELS:

- Architectural/Algorithmic level.
- Dataflow level.
- Gate level.
- Switch level.

SOFTWARE:

- Xilinx.

Version:

- 12.4i

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Sample IEEE VHDL Projects Topics.

SI	IEEE VHDL Projects Titles.
1	A novel VHDL implementation of UART with single error correction and double error detection capability.
2	Analysis of effects of using exponent adders in IEEE-754 multiplier by VHDL.
3	Implementation using VHDL of an ECG signal using CSP.
4	Deadlock detection in FPGA design: A practical approach.
5	Integrated Circuit Modeling for Noise Susceptibility Prediction in Communication Networks.
6	Real time implementation of a novel chaotic generator on FPGA.
7	Vehicle parking system implementation using CPLD.
8	Edge dedection application with FPGA based Sobel operator.
9	Comparisions of Robert, Prewitt, Sobel operator based edge detection methods for real time uses on FPGA.
10	Complex-multiplier implementation for pipelined FFTs in FPGAs.
11	An iLab for Teaching Advanced Logic Concepts With Hardware Descriptive Languages.
12	Implementation of adaptive noise canceller using FPGA for real-time applications.
13	Implementation of AES algorithm on FPGA for low area consumption.
14	Addition of redundant Binary Signed Digits using RBSD adder.
15	Implementation of NB PHY transceiver of IEEE 802.15.6 WBAN on FPGA.
16	IR and LASER sensors for Newtonian fluids for flow-rate measurement using FPGA.
17	Area-high speed design trade-offs for advanced encryption standard cipher engine.
18	Comparative Design and Synthesis of IR and Optical Sensors for Fluid Flowrate Using FPGA.
19	PVT variations of a behaviorally modeled single walled carbon nanotube field-effect transistor (SW-CNTFET).
20	Towards 32-bit Energy-Efficient Superconductor RQL Processors: The Cell-Level Design and Analysis of Key Processing and On-Chip Storage Units.
21	750-kW interleaved buck converter dc supply control implementation in a low-cost FPGA.
22	Electro-thermal virtual prototyping of a Rogowski Coil sensor system.
23	Parallel H.264/AVC Fast Rate-Distortion Optimized Motion Estimation by Using a Graphics Processing Unit and Dedicated Hardware.
24	Low complexity modified constant Log-Map algorithm for radix-4 turbo decoder.

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25	Electrical predictive model of Zener diode under pulsed EOS.
26	Physical level IC implementation for speed control of three phase induction motors.
27	Functional Constraint Extraction From Register Transfer Level for ATPG.
28	Electro-thermal modeling of a Rogowski coil sensor system.
29	DELPHI: a framework for RTL-based architecture design evaluation using DSENT models.
30	Design and analysis of ALU: Vedic mathematics approach.
31	Power Loss Prediction and Precise Modeling of Magnetic Powder Components in DC–DC Power Converter Application.
32	Design and Experimental Implementation of DTC of an Induction Machine Based on Fuzzy Logic Control on FPGA.
33	Multiplier-less pipeline architecture for lifting-based two-dimensional discrete wavelet transform.
34	Evaluation of testability of digital circuits by fault injection technique.
35	C1. Flexible LDPC decoder architecture for (3–6) regular codes.
36	Rapid prototyping of FPGA based digital controller of DSTATCOM for load compensation under distorted utility condition.
37	A Matlab/Simulink model for multi-scroll chaotic attractors.
38	HDLs evolve as they affect design methodology for a higher abstraction and a better integration.
39	Hardware architectures for the H.265/HEVC discrete cosine transform.
40	An Approach for Side Scan Sonar Acoustic Images Segmentation using Programmable Logic.
41	Rapid-X - An FPGA Development Toolset Using a Custom Simulink Library for MTCA.4 Modules.
42	Design and implementation of 16 × 16 multiplier using Vedic mathematics.
43	Implementation of High Speed Matrix Multiplier Using Vedic Mathematics on FPGA.
44	RFID UHF protocol implementation in distributed sensor networks.
45	Nexus#: A Distributed Hardware Task Manager for Task-Based Programming Models.
46	Hardware implemented adaptive neuro fuzzy system.
47	Basic Programmable Logic controller with FPGA and Artificial Neural Networks.
48	High frequency characterization and modeling via measurements of power electronic capacitors under high bias voltage and temperature variations.
49	Transparent linking of compiled software and synthesized hardware.
50	Design of Mixed Synchronous/Asynchronous Systems with Multiple Clocks.